REMARKS

This response responds to the Office Action dated June 28, 2005 in which the Examiner rejected claims 1-4 under 35 U.S.C. §103.

Claim 1 claims a serial-data-communication apparatus and claims 3 claims a method of detecting a communication error in transmission and reception of serial data composed of a plurality of bits including a start bit at a head. The apparatus and method comprised an edge-detecting means, start-bit-level-inspection means and start-bit-detection-error-notification means. The edge-detection means is for detecting a trailing edge of received data. The start-bit-level-inspection means is for recognizing the reception of the start bit of the received data based upon the detection of the trailing edge provided by the edge-detection means, and is for monitoring a bit level of the start bit to examine whether the start bit maintains a predetermined bit level. The start-bit-detection-error-notification means outputs a signal to an external circuit which indicates occurrence of an error in detecting the start bit, when any change in the bit level of the start bit is detected by the start-bit-level-inspection means.

Through the structure and method of the claimed invention outputting a signal indicating when any change in the bit level of a start bit is detected as claimed in claims 1 and 3, the claimed invention provides a serial-data-communication apparatus and method in which any problem relating to the start bit error is immediately discovered so that the time for recovery can be reduced. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 3.

Claims 1-4 were rejected under 35 U.S.C. §103 as being unpatentable over *Ito* (U.S. Patent No. 5,623,522) in view of *Davis et al.* (U.S. Patent No. 5,263,054) and further in view of *Asano et al.* (U.S. Patent No. 5,636,343).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Ito appears to disclose asynchronous serial data receiving devices which operate based on start-stop-synchronization communication method (or asynchronous communication method). (col. 1, lines 7-10) FIG. 1 shows a configuration of an asynchronous serial data receiving device 1. The device 1 is configured by a first shift register circuit 2, a clock circuit 8, a counter circuit 4, a decoder circuit 5, a second shift register circuit 6, a latch circuit 7, an edge detecting circuit 8, a window signal circuit 9, a flag signal circuit 10 and a logical gate 11. Herein, the first shift register circuit 2 receives input serial data transmitted thereto; the clock circuit 8 produces high-speed clocks, whose speed is higher than a bit rate of the input serial data, as system clocks; the counter circuit 4 counts number of the system clocks outputted from the clock circuit 3; the decoder circuit 5 produces a variety of signals based on a count number of the counter circuit 4; the second shift register circuit 6 receives serial data, from the first shift register circuit 2, which are delayed behind the input serial data by `n` clocks; the latch circuit 7 extracts and latches parallel data from the second shift register circuit 6; and the edge detecting circuit 8 detects a trailing edge of the input serial data received by the first shift register circuit 2. In addition, the window signal circuit 9 produces a window signal;

and the flag signal circuit 10 produces a flag signal. The logical gate 11 produces a RESET signal which resets the window signal and flag signal. (col. 2, line 63 through col. 3, line 19) Due to occurrence of the noise A, the edge detecting circuit 8 cannot detect a trailing edge of the start bit S at a moment t11. The edge detecting circuit 8 detects the trailing edge at a moment t12 at which the noise A disappears. So, the edge detecting circuit 8 produces a SET signal, which is delivered to the window signal circuit 9 and the flag signal circuit 10. Thus, the asynchronous serial data receiving device 1 performs the aforementioned operations, so that the decoder circuit 5 produces a shift clock. Due to the noise A, the decoder circuit 5 forms a leading-edge timing of the shift clock at a timing `a1` which is delayed behind a change point between consecutive bits of the 7.5-clock-delayed serial data, wherein the timing a1 is further delayed as compared to a normal leading-edge timing of the shift clock which is produced under a normal state where noise does not occur. Even if the leading-edge timing of the shift pulse is further delayed because of occurrence of the noise A, the device 1 works well so that bits b1 to b8 of main data are sequentially read out and stored, with being shifted, in the second shift register circuit 6. (col. 7, lines 37-57)

Thus, *Ito* merely discloses an edge detecting circuit 8 which detects the trailing edge of an input serial data which is delayed by one clock. Nothing in *Ito* shows, teaches or suggests a) monitoring a bit level of a start bit to examine whether the start bit maintains a predetermined bit level or b) outputting a signal to an external circuit when any change of the bit level of the start bit is detected as claimed in claims 1 and 3. Rather, *Ito* merely discloses an edge detecting circuit at 8 detecting the trailing edge of a delayed signal.

Davis et al. appears to disclose method and system for efficient non-coherent demodulation of frequency shift keyed signals by reducing the rate of computation required from a demodulation process on a digital signal processor. (col. 1, lines 23-27) Whether a valid start bit has been found is then verified by checking that the level continues to correspond to a start bit level (logic 0). As a result, subsequent delays of one bit period should provide samples at the center of each subsequent bit period. This sampling continues until all of the bits in the current word have been detected, including the stop bits. Then, searching for another start bit begins. When a start bit is detected, linear interpolation is utilized to determine the time delay between the demodulator computation and the actual threshold crossing. A supplemental delay period is added to the delay in order to step to the point in time corresponding to the center of the start bit. (col. 4, line 58 through col. 5, line 3)

Thus, *Davis et al.* merely discloses determining whether a valid start bit has been found by verifying that the level continues to correspond to a start bit level in order to utilize linear interpolation. (col. 4, lines 66-67) Nothing in *Davis et al.* shows, teaches or suggests outputting a signal to an external circuit indicating the occurrence of error when any change of a bit level of a start bit is detected as claimed in claims 1 and 3. Rather, *Davis et al.* merely discloses determining if a valid start bit has been found in order to utilize linear interpolation.

Asano et al. appears to disclose a microcomputer which comprises a built-in serial input-output circuit which outputs data in converting parallel data into serial data and converts input serial data into parallel data. (col. 1, lines 9-12) In a transmitting period, when discordance occurs between a signal at the R.X.D terminal and a signal at the T X D terminal, the output of the exclusive-OR circuit 1 is raised

to a high level. Then the output of the D flip-flop circuit 2 is made high, and an interrupt signal is given to the CPU 101. As mentioned in the above, the discordance between the signal at the R X D terminal and the signal at the T X D terminal can be detected without comparing these signals by software. In the result, the load on the software is lightened. In other words, the time to be shared for other processes, a protocol control process, for example, can be increased, so that even if a data transfer speed is made high, the transmitting-receiving process can be executed. (col. 5, lines 13-25)

Thus, *Asano et al.* merely discloses that when discordance occurs between two signals, an interrupt signal is given to CPU (col. 5 lines 14-17). Nothing in *Asano et al.* shows, teaches or suggests outputting an error signal when any change in the bit level of the start bit is detected as claimed in claims 1 and 3. Rather, *Asano et al.* merely discloses outputting an interrupt when a discordance between two signals is detected.

A combination of *Ito*, *Davis et al.* and *Asano et al.* would merely suggest to detect the trailing edge of a delayed signal as taught by *Ito,* determining if a valid start bit is found in order to utilize linear interpolation as taught by *Davis et al.* and to output an interrupt signal when a discordance occurs between two signals as taught by *Asano et al.* Thus nothing in the combination of *Ito*, *Davis et al.* and *Asano et al.* show, teach or suggest outputting an error signal to an external circuit when any change in the bit level of a start bit is detected as claimed in claims 1 and 3. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 3 under 35 U.S.C. §103.

Claims 2 and 4 depend from claims 1 and 3 and recite additional features. Applicant respectfully submits that claims 2 and 4 would not have been obvious within the meaning of 35 U.S.C. §103 over *Setoguchi et al.* and *Asano et al.* at least for the reasons as set forth above with respect to claims 1 and 3. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2 and 4 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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